UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,159	03/30/2001	Sheng Zhao	871.0013USU	8117

29683 7590 07/26/2005

HARRINGTON & SMITH, LLP
4 RESEARCH DRIVE
SHELTON, CT 06484-6212

EXAMINER	
PATEL, NIMESH G	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 07/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,159	ZHAO ET AL.	
	Examiner	Art Unit	
	Nimesh G. Patel	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9,11-17 and 19-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9,11-17 and 19-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 23-24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In this case, the specification does not disclose a wireless communication device.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1,3, 5-9, 11, 13-17, 19, and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Earnest('338), in view of what is well known in the art, as evidenced by Sato('149), and in further view of Veenstra('946).

5. Regarding claim 1, Earnest discloses a programmable buffer circuit for interfacing a CPU to a plurality of channel interfaces comprising of a dual port memory(Figure 3, Block 100), an arbitrator for arbitrating access to the dual port memory(Column 3, Lines 53-54; A higher priority channel can interrupt service and therefore would indicate an arbitrator to arbitrate access to the memory.), an address generator

for addressing the dual port memory(Column 5, Lines 59-65), and an allocator and control unit for specifying buffer locations for individual channels(Column 3, Lines 3-15).

Earnest discloses multiple dual port memories instead of a single dual port memory. Making something integral, such as multiple memories into a single memory, is not a patentable concept(See MPEP 2144.04.V.B), since a combination of the multiple memories of Earnest into a single dual port memory would operate in the same manner as the dual port memory claimed in the application. As further evidence, Sato discloses the replacement of two RAMs with a single dual port memory(Column 25, Lines 5-10).

Earnest does not specifically disclose a first case, wherein the control unit operates individual ones of channel buffers in a block access mode of operation using a set of channel registers and a second case, wherein the control unit operates said individual ones of channel buffers in a first in, first out (FIFO) access mode of operation using said same set of channel registers. However, Veenstra discloses memory in block access mode(RAM mode) and in FIFO mode(Column 7, Lines 27-35) using same set of registers(column 9, Lines 20-32). Therefore it would have been obvious to use the ram in multiple modes of operations using same set of registers, as disclosed by Veenstra, in the system of Earnest, for the advantage of saving space.

6. Regarding claim 3, Earnest discloses an integrated circuit containing a dual port memory, CPU, and plurality of interface channels (Column 2, Lines 45-50).

7. Regarding claim 5, Earnest discloses an interface channel comprising of a serial data interface(Column 5, Line 3).

8. Regarding claim 6, Earnest discloses an interface channel comprising of a packet data interface(Column 5, Lines 4-6).

9. Regarding claim 7, Earnest discloses plurality of channels comprising of receive and transmit interfaces(Column 4, Lines 56-63) and an allocator comprising registers for specifying the starting address and size for each of the receive and transmit interfaces(Column 3, Lines 3-15).

10. Regarding claim 8, Earnest discloses plurality of channels comprising of receive and transmit interfaces(Column 4, Lines 56-63) and a receive buffer of one channel interface to be a transmit buffer of another channel(Column 4, Lines 20-23).

11. Regarding claim 9, Earnest discloses a dual port memory couple to a CPU data bus and to a channel data bus that serves a plurality of channel interfaces(Figure 2), programming a control unit for specifying a set of channel registers individual ones of buffer locations and sizes within a dual port memory for the channel interfaces(Column 3, Lines 3-15), and arbitrating for access to the dual port memory(Column 3, Lines 53-54). Earnest further discloses the generation of dual port memory address depending on what channel interface is currently selected and on the specified buffer location and size for that channel interface(Column 7, Lines 28-48).

Earnest discloses multiple dual port memories instead of a single dual port memory. Making something integral, such as multiple memories into a single memory, is not a patentable concept(See MPEP 2144.04.V.B), since a combination of the multiple memories of Earnest into a single dual port memory would operate in the same manner as the dual port memory claimed in the application. As further evidence, Sato discloses the replacement of two RAMs with a single dual port memory(Column 25, Lines 5-10).

Earnest does not specifically disclose a first case, wherein the control unit operates individual ones of channel buffers in a block access mode of operation using a set of channel registers and a second case, wherein the control unit operates said individual ones of channel buffers in a first in, first out (FIFO) access mode of operation using said same set of channel registers. However, Veenstra discloses memory in block access mode(RAM mode) and in FIFO mode(Column 7, Lines 27-35) using same set of

registers(column 9, Lines 20-32). Therefore it would have been obvious to use the ram in multiple modes of operations using same set of registers, as disclosed by Veenstra, in the system of Earnest, for the advantage of saving space.

12. Regarding claim 11, Earnest discloses an integrated circuit containing a dual port memory, CPU, and plurality of interface channels (Column 2, Lines 45-50).

13. Regarding claim 13, Earnest discloses plurality of channels comprising of receive and transmit interfaces(Column 4, Lines 56-63) and specifying the starting address and size for each of the receive and transmit interfaces(Column 3, Lines 3-15).

14. Regarding claim 14, Earnest discloses plurality of channels comprising of receive and transmit interfaces(Column 4, Lines 56-63) and a receive buffer of one channel interface to be a transmit buffer of another channel(Column 4, Lines 20-23).

15. Regarding claim 15, Earnest discloses a programmable buffer circuit for interfacing a data processor to a plurality of channel interfaces comprising of a dual port memory(Figure 3, Block 100), an arbitrator for arbitrating access to the dual port memory(Column 3, Lines 53-54; A higher priority channel can interrupt service and therefore would indicate an arbitrator to arbitrate access to the memory.), an address generator for addressing the dual port memory(Column 5, Lines 59-65), and a control unit for specifying buffer locations for individual channels(Column 3, Lines 3-15). Earnest further discloses a control unit to be programmable for operating individual ones of channel buffers in FIFO access mode of operation(Column 3, Lines 3-15).

Earnest discloses multiple dual port memories instead of a single dual port memory. Making something integral, such as multiple memories into a single memory, is not a patentable concept(See MPEP 2144.04.V.B), since a combination of the multiple memories of Earnest into a single dual port memory would operate in the same manner as the dual port memory claimed in the application. As further

evidence, Sato discloses the replacement of two RAMs with a single dual port memory(Column 25, Lines 5-10).

Earnest does not specifically disclose a first case, wherein the control unit operates individual ones of channel buffers in a block access mode of operation using a set of channel registers and a second case, wherein the control unit operates said individual ones of channel buffers in a first in, first out (FIFO) access mode of operation using said same set of channel registers. However, Veenstra discloses memory in block access mode(RAM mode) and in FIFO mode(Column 7, Lines 27-35) using same set of registers(column 9, Lines 20-32). Therefore it would have been obvious to use the ram in multiple modes of operations using same set of registers, as disclosed by Veenstra, in the system of Earnest, for the advantage of saving space.

16. Regarding claim 16, Earnest discloses plurality of channels comprising of receive and transmit interfaces(Column 4, Lines 56-63) and a receive buffer of one channel interface to be a transmit buffer of another channel(Column 4, Lines 20-23).

17. Regarding claim 17, Earnest discloses a programmable buffer circuit for interfacing a data processor to a plurality of channel interfaces comprising of a dual port memory(Figure 3, Block 100), an arbitrator for arbitrating access to the dual port memory(Column 3, Lines 53-54; A higher priority channel can interrupt service and therefore would indicate an arbitrator to arbitrate access to the memory.), an address generator for addressing the dual port memory(Column 5, Lines 59-65), and a control unit for specifying buffer locations for individual channels(Column 3, Lines 3-15), where control unit is responsive to operate in a FIFO mode(Column 3, Lines 3-15).

Earnest does not specifically disclose four transmit registers allocated for each channel designated as BaseReg0, BaseReg1, SizeReg0, and SizeReg1 and four receive registers also designated as BaseReg0, BaseReg1, SizeReg0, and SizeReg1. However, Earnest does show pointers, i.e. registers, to perform the functions of the registers BaseReg0, BaseReg1, SizeReg0, SizeReg1(Column 7, Lines 16-47; For

Transmit purposes, TxQ_PARMS is used to set the size of the individual buffers, performing the function of the Size registers, and WR_PNTR is used for the starting address of the individual channels, performing the function of the Base Registers.).

Earnest does not specifically disclose a first case, wherein the control unit operates individual ones of channel buffers in a block access mode of operation using a set of channel registers and a second case, wherein the control unit operates said individual ones of channel buffers in a first in, first out (FIFO) access mode of operation using said same set of channel registers. However, Veenstra discloses memory in block access mode(RAM mode) and in FIFO mode(Column 7, Lines 27-35) using same set of registers(column 9, Lines 20-32). Therefore it would have been obvious to use the ram in multiple modes of operations using same set of registers, as disclosed by Veenstra, in the system of Earnest, for the advantage of saving space. Earnest further discloses generating a FULL flag(Column 11, Line 40) indicating a High Threshold Register being used and an EMPTY flag(Column 8, line 58) indicating a Low Threshold Register being used.

18. Regarding claim 19, Earnest discloses a programmable buffer circuit for interfacing a data processor to a plurality of channel interfaces comprising of a dual port memory(Figure 3, Block 100), an arbitrator for arbitrating access to the dual port memory(Column 3, Lines 53-54; A higher priority channel can interrupt service and therefore would indicate an arbitrator to arbitrate access to the memory.), an address generator for addressing the dual port memory(Column 5, Lines 59-65), and a control unit for specifying buffer locations for individual channels(Column 3, Lines 3-15). Earnest further discloses a control unit to be programmable for operating individual ones of channel buffers in FIFO access mode of operation(Column 3, Lines 3-15).

Earnest does not specifically disclose a first case, wherein the control unit operates individual ones of channel buffers in a block access mode of operation using a set of channel registers and a second case, wherein the control unit operates said individual ones of channel buffers in a first in, first out (FIFO)

access mode of operation using said same set of channel registers. However, Veenstra discloses memory in block access mode(RAM mode) and in FIFO mode(Column 7, Lines 27-35) using same set of registers(column 9, Lines 20-32). Therefore it would have been obvious to use the ram in multiple modes of operations using same set of registers, as disclosed by Veenstra, in the system of Earnest, for the advantage of saving space.

19. Regarding claim 21, Earnest discloses a programmable buffer circuit for interfacing a CPU to a plurality of channel interfaces comprising of a dual port memory(Figure 3, Block 100), means for arbitrating access to the dual port memory(Column 3, Lines 53-54; A higher priority channel can interrupt service and therefore would indicate an arbitrator to arbitrate access to the memory.), means for generating dual port memory addresses(Column 5, Lines 59-65), and means for allocating and means for controlling, programmable by said CPU for specifying buffer locations for individual channels(Column 3, Lines 3-15).

Earnest discloses multiple dual port memories instead of a single dual port memory. Making something integral, such as multiple memories into a single memory, is not a patentable concept(See MPEP 2144.04.V.B), since a combination of the multiple memories of Earnest into a single dual port memory would operate in the same manner as the dual port memory claimed in the application. As further evidence, Sato discloses the replacement of two RAMs with a single dual port memory(Column 25, Lines 5-10).

Earnest does not specifically disclose a first case, wherein the control unit operates individual ones of channel buffers in a block access mode of operation using a set of channel registers and a second case, wherein the control unit operates said individual ones of channel buffers in a first in, first out (FIFO) access mode of operation using said same set of channel registers. However, Veenstra discloses memory in block access mode(RAM mode) and in FIFO mode(Column 7, Lines 27-35) using same set of registers(column 9, Lines 20-32). Therefore it would have been obvious to use the ram in multiple modes

of operations using same set of registers, as disclosed by Veenstra, in the system of Earnest, for the advantage of saving space.

20. Regarding claim 22, Earnest discloses an integrated circuit containing a dual port memory, CPU, and plurality of interface channels (Column 2, Lines 45-50).

21. Regarding claims 23-24, they are rejected on the same grounds of rejection as claim 1. Earnest and Veenstra do not specifically disclose a wireless communication device. However, Official Notice is being taken that wireless communication devices are well known in the art and it would be obvious to use the system of Earnest and Veenstra in a wireless communication device since this is newer technology and the convenience of wireless devices.

22. Claims 4, 12 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Earnest in view of Veenstra, and in further view of Begur et al.('649).

23. Regarding claim 4, Earnest and Veenstra do not specifically disclose a channel interface as an audio codec. However, Earnest discloses example data interface circuits and discloses other types of data interface controllers also can be used(Column 5, Lines 2-10). Begur discloses a circuit with plurality of interface channels with an audio codec channel(Column 6, Lines 55-60). Therefore it would have been obvious to one of an ordinary skill in the art to include the audio codec of Begur in the system of Earnest and Veenstra for the purpose of handling an audio stream that needs to be encoded/decoded.

24. Regarding claim 12, Earnest discloses an interface channel comprising of a packet data interface and a serial data interface(Column 5, Lines 4-6).

Earnest and Veenstra do not specifically disclose a channel interface as an audio codec. However, Earnest discloses example data interface circuits and discloses other types of data interface controllers also can be used(Column 5, Lines 2-10). Begur discloses a circuit with plurality of interface channels with an audio codec channel(Column 6, Lines 55-60). Therefore it would have been obvious to one of an

ordinary skill in the art to include the audio codec of Begur in the system of Earnest and Veenstra for the purpose of handling an audio stream that needs to be encoded/decoded.

25. Regarding claim 20, Earnest discloses an interface channel comprising of a packet data interface(Column 5, Lines 4-6).

Earnest does not specifically disclose a channel interface as an audio codec. However, Earnest discloses example data interface circuits and discloses other types of data interface controllers also can be used(Column 5, Lines 2-10). Begur discloses a circuit with plurality of interface channels with an audio codec channel(Column 6, Lines 55-60). Therefore it would have been obvious to one of an ordinary skill in the art to include the audio codec of Begur in Earnest's system for the purpose of handling an audio stream that needs to be encoded/decoded.

Response to Arguments

26. Applicant's arguments with respect to claim1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

27. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nimesh G. Patel whose telephone number is 571-272-3640. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nimesh G Patel
Examiner
Art Unit 2112

NP
July 25, 2005

TIM VO
PRIMARY EXAMINER